The invention claimed is:

1. A interconnecting element structure, comprising:

an array of elements; and

a plurality of connection path segments, wherein:

each connection path segment links two of the elements;

the elements include edge elements and interior elements;

the array is substantially arranged in rows of elements and columns of elements;

each segment in a first subset of the connection path segments links one interior element in the array to another interior element in the array, while each segment in a second subset of the connection path segments links an interior element in the array to an edge element in the array; and

at least a majority of the segments in the first subset do not link interior elements that are nearest neighbors to each other in the array.

2. The structure of claim 1 wherein each segment in a third subset of the connection path segments links an edge element in the array to an external element.

3. The structure of claim 1 wherein:

the connection path segments are arranged such that a group of the segments forms an overall, continuous connection path for at least one of the columns; and

the connection path segments are arranged such that a group of the segments forms an overall, continuous connection path for at least one of the rows.

4. The structure of claim 3 wherein the overall, continuous connection path for at least one column or row includes an element that is external to the array.

5. The structure of claim 1 wherein at least a majority of the segments in the first subset link alternating interior elements in the array.

6. The structure of claim 1 wherein the connection path segments are further arranged to provide an overall, continuous connection path for at least one diagonal line of elements in the array.

7. The structure of claim 1 wherein the elements are semiconductor logic elements.

8. The structure of claim 1 wherein the elements are nodes in a neural network.

9. The structure of claim 1 wherein the segments transfer data to the elements.

10. The structure of claim 1 wherein the segments transfer one or more commands to the elements.

11. The structure of claim 1 wherein the segments transfer one or more addresses to the elements.

12. The structure of claim 1 wherein the connection path segments comprise electrically conductive busses.

13. The structure of claim 1 further comprising an electrically conductive bus that delivers one or more of data, commands and addresses to the connection path segments.

14. The structure of claim 3 wherein the overall, continuous connection path for at least one of the columns is symmetrical.

15. The structure of claim 3 wherein the overall, continuous connection path for at least one of the rows is symmetrical.

16. The structure of claim 6 wherein the connection path for at least one of the diagonal lines is symmetrical.

17. A conductive structure, comprising:

an array of elements; and

a plurality of connection path segments, wherein:

each connection path segment links two of the elements;

the elements include edge elements and interior elements;

the array is substantially arranged in rows of elements and columns of elements; and

no connection path segment links one edge element in a row or column of the array to another edge element in the same row or column of the array.

18. The structure of claim 17 wherein:

the connection path segments are arranged such that a group of the segments forms an overall, continuous connection path for at least one of the columns; and

the connection path segments are arranged such that a group of the segments forms an overall, continuous connection path for at least one of the rows.

19. The structure of claim 18 wherein the overall, continuous connection path for at least one column or row includes an element that is external to the array.

20. The structure of claim 17 wherein at least a majority of the segments link alternating interior elements in the array.

21. The structure of claim 17 wherein the connection path segments are further arranged to provide an overall, continuous connection path for at least one diagonal line of elements in the array.

22. The structure of claim 17 wherein the elements are semiconductor logic elements.

23. The structure of claim 17 wherein the elements are nodes in a neural network.

24. The structure of claim 17 wherein the segments transfer data to the elements.

25. The structure of claim 17 wherein the segments transfer one or more commands to the elements.

26. The structure of claim 17 wherein the segments transfer one or more addresses to the elements.

27. The structure of claim 17 wherein the connection path segments comprise electrically conductive busses.

28. The structure of claim 17 further comprising an electrically conductive bus that delivers one or more of data, commands and addresses to the connection path segments.

29. The structure of claim 18 wherein the overall, continuous connection path for at least one of the columns is symmetrical.

30. The structure of claim 18 wherein the overall, continuous connection path for at least one of the rows is symmetrical.

31. The structure of claim 21 wherein the connection path for at least one of the diagonal lines is symmetrical.

32. A conductive structure, comprising:

a symmetrical array of elements; and

a plurality of connection path segments, wherein:

each connection path segment links two of the elements;

the elements include edge elements and interior elements; and

each segment that links one interior element in the structure to another interior element in the structure has a length that is at least as large as the distance between three elements in the array.

33. The structure of claim 32 wherein:

the array is substantially arranged in rows of elements and columns of elements;

the connection path segments are arranged such that a group of the segments forms an overall, continuous connection path for at least one of the columns; and

the connection path segments are arranged such that a group of the segments forms an overall, continuous connection path for at least one of the rows.

34. The structure of claim 33 wherein the overall, continuous connection path for at least one column or row includes an element that is external to the array.

35. The structure of claim 32 wherein at least a majority of the segments link alternating interior elements in the array.

36. The structure of claim 32 wherein the connection path segments are further arranged to provide an overall, continuous connection path for at least one diagonal line of elements in the array.

37. The structure of claim 32 wherein the elements are semiconductor logic elements.

38. The structure of claim 32 wherein the elements are nodes in a neural network.

39. The structure of claim 32 wherein the segments transfer data to the elements.

40. The structure of claim 32 wherein the segments transfer one or more commands to the elements.

41. The structure of claim 32 wherein the segments transfer one or more addresses to the elements.

42. The structure of claim 32 wherein the connection path segments comprise electrically conductive busses.

43. The structure of claim 32 further comprising an electrically conductive bus that delivers one or more of data, commands and addresses to the connection path segments.

44. The structure of claim 33 wherein the overall, continuous connection path for at least one of the columns is symmetrical.

45. The structure of claim 33 wherein the overall, continuous connection path for at least one of the rows is symmetrical.

46. The structure of claim 36 wherein the connection path for at least one of the diagonal lines is symmetrical.